FLIPPER: in Rad-Test Veritas

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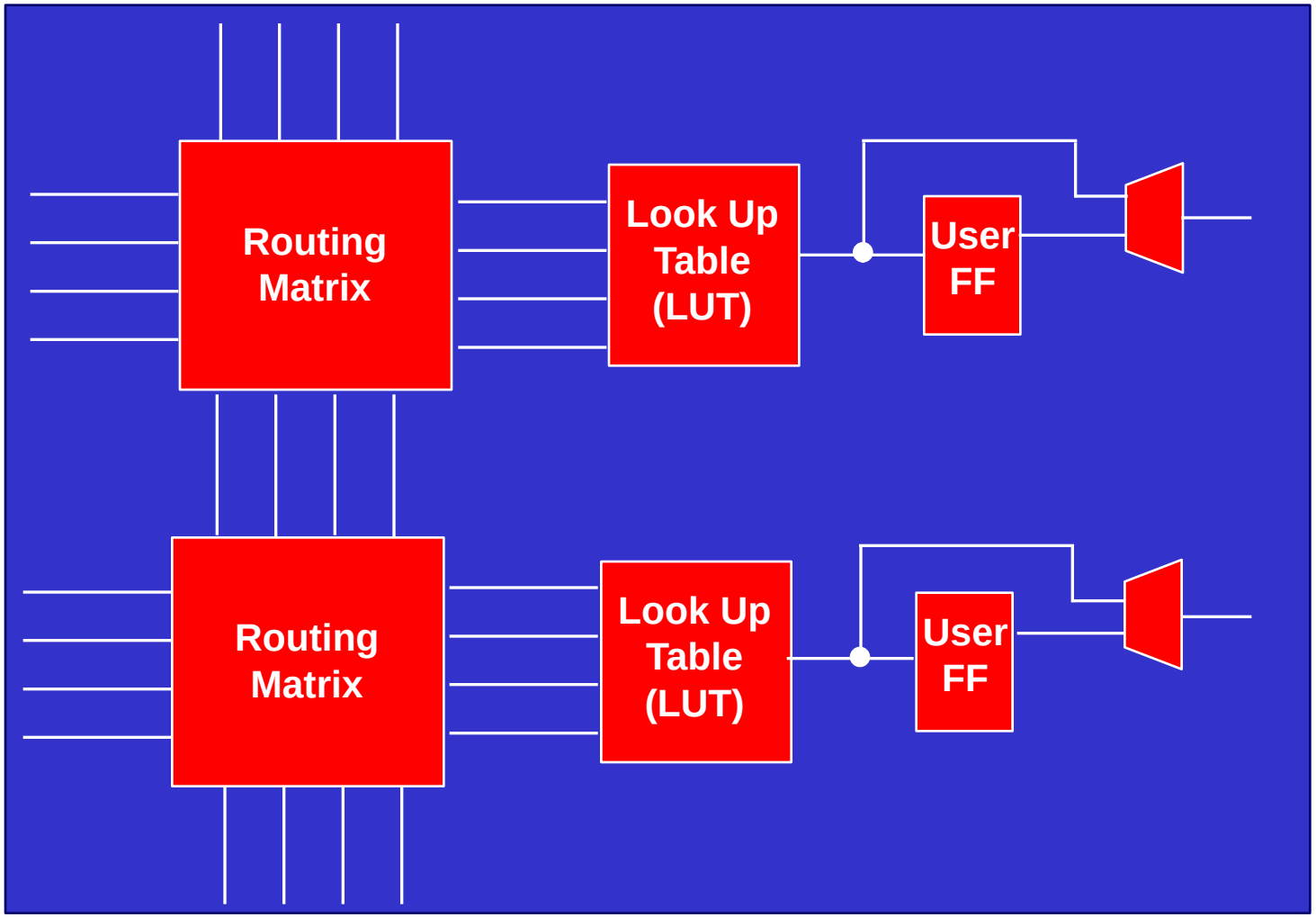
Astro-Siesta, 20/01/2011

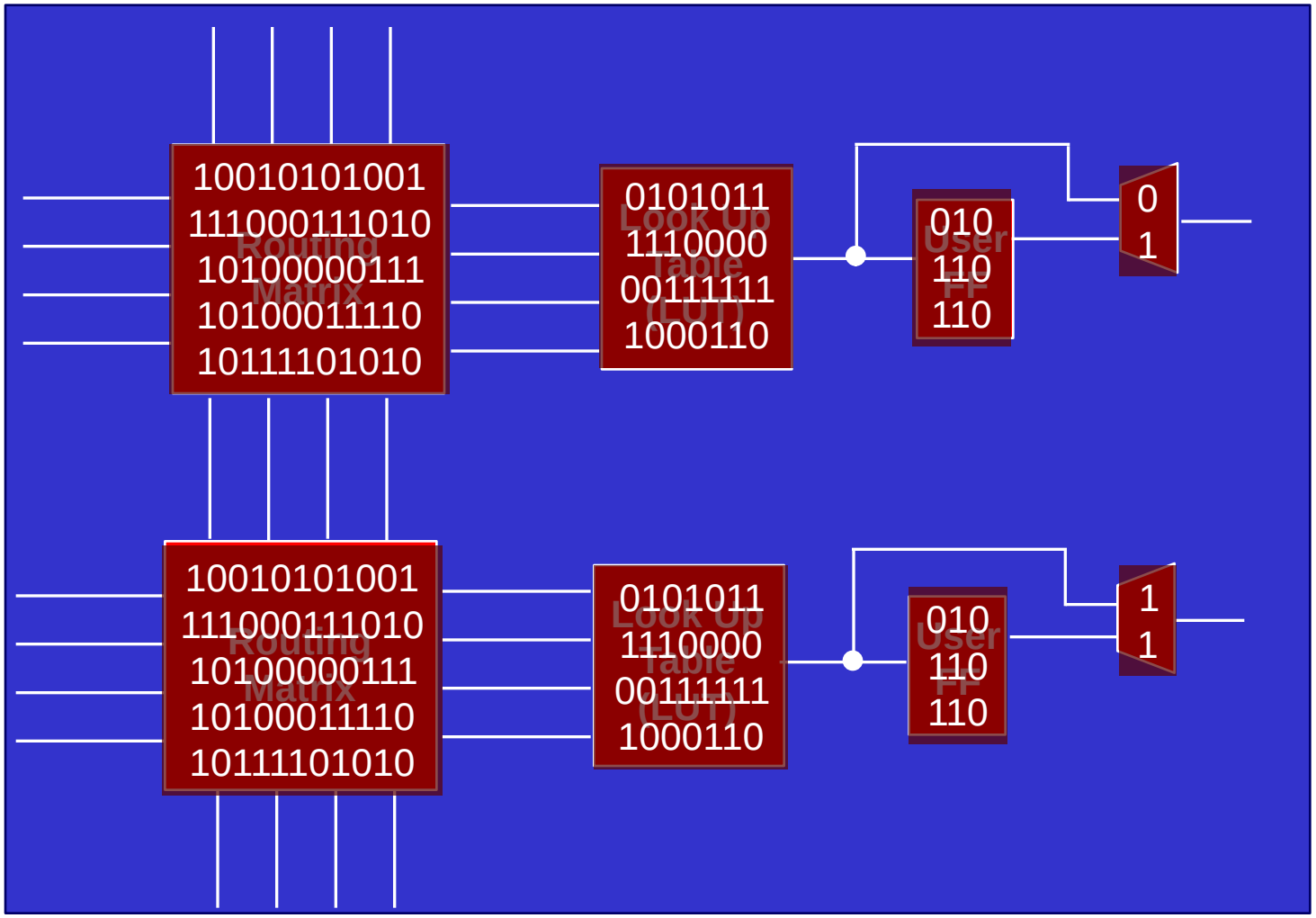
Introducing SRAM-FPGAs…

- FPGAs can be customized
  - Can be faster and more efficient than a "standard" processor
  - Provide a high density logic (over 1 million gates)
- FPGAs are reprogrammable
  - FPGA resources can be used for multiple instruments and missions
  - Errors in an FGA design can be repaired in orbit

SRAM-FPGAS Architecture



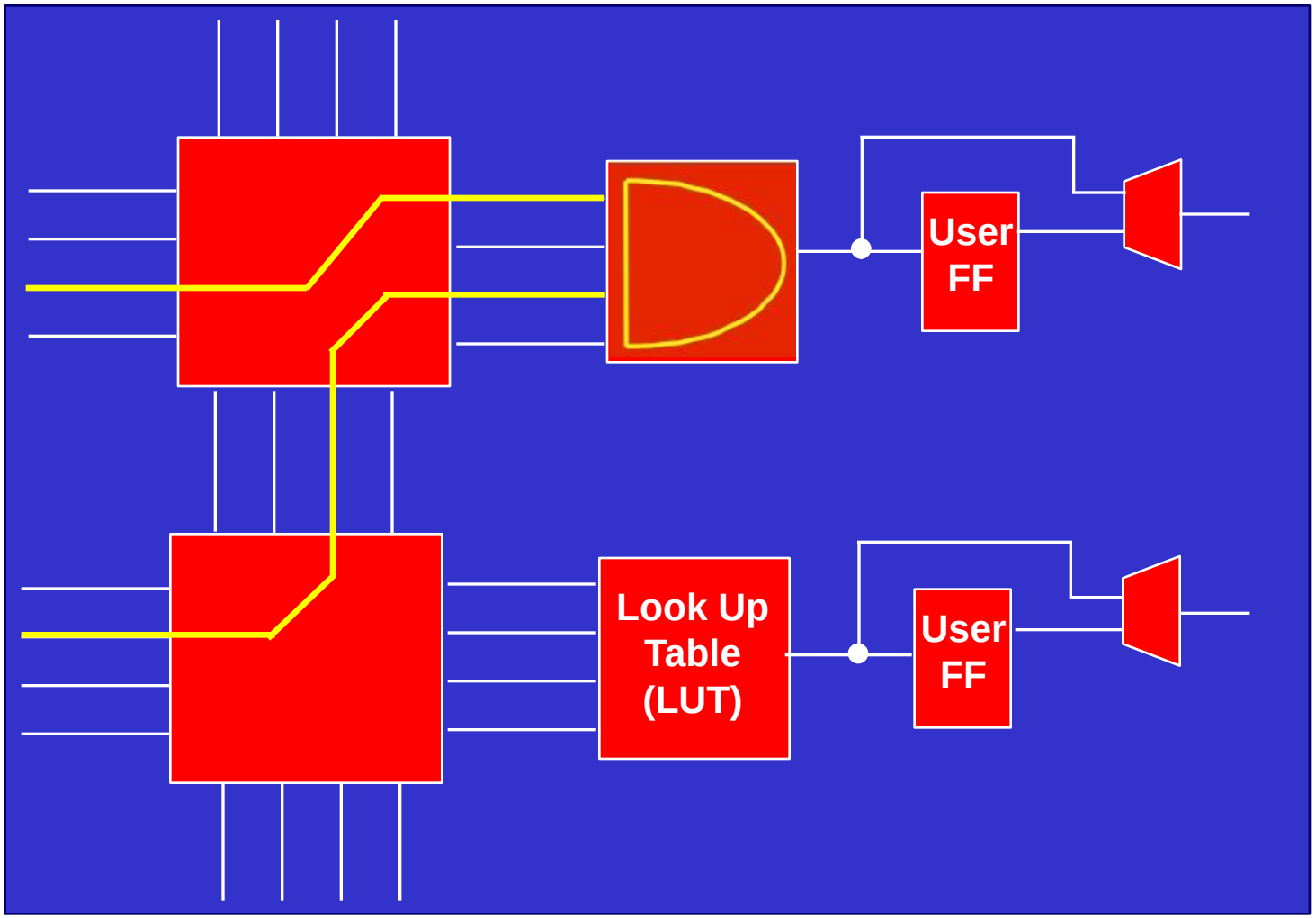
SRAM-FPGAs Configuration Bits



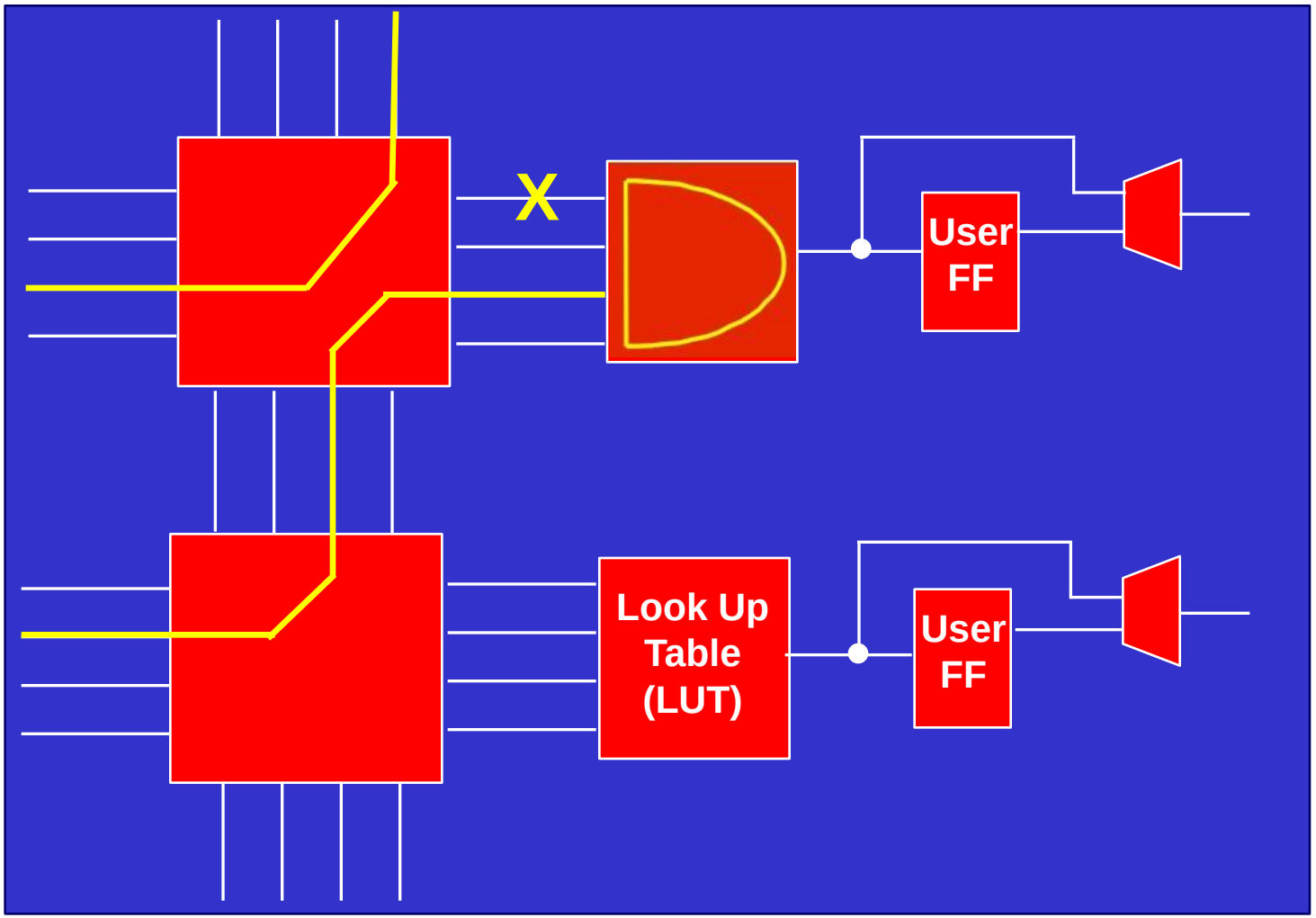
SRAM-FPGA Radiation Sensitivity

- Single Event Upset (SEU) from Heavy Ions and Protons
- SEU in SRAM-FPGAs affect
  - Flip-flops
  - User memory
  - Configuration memory and thus the logical function of the circuit as well

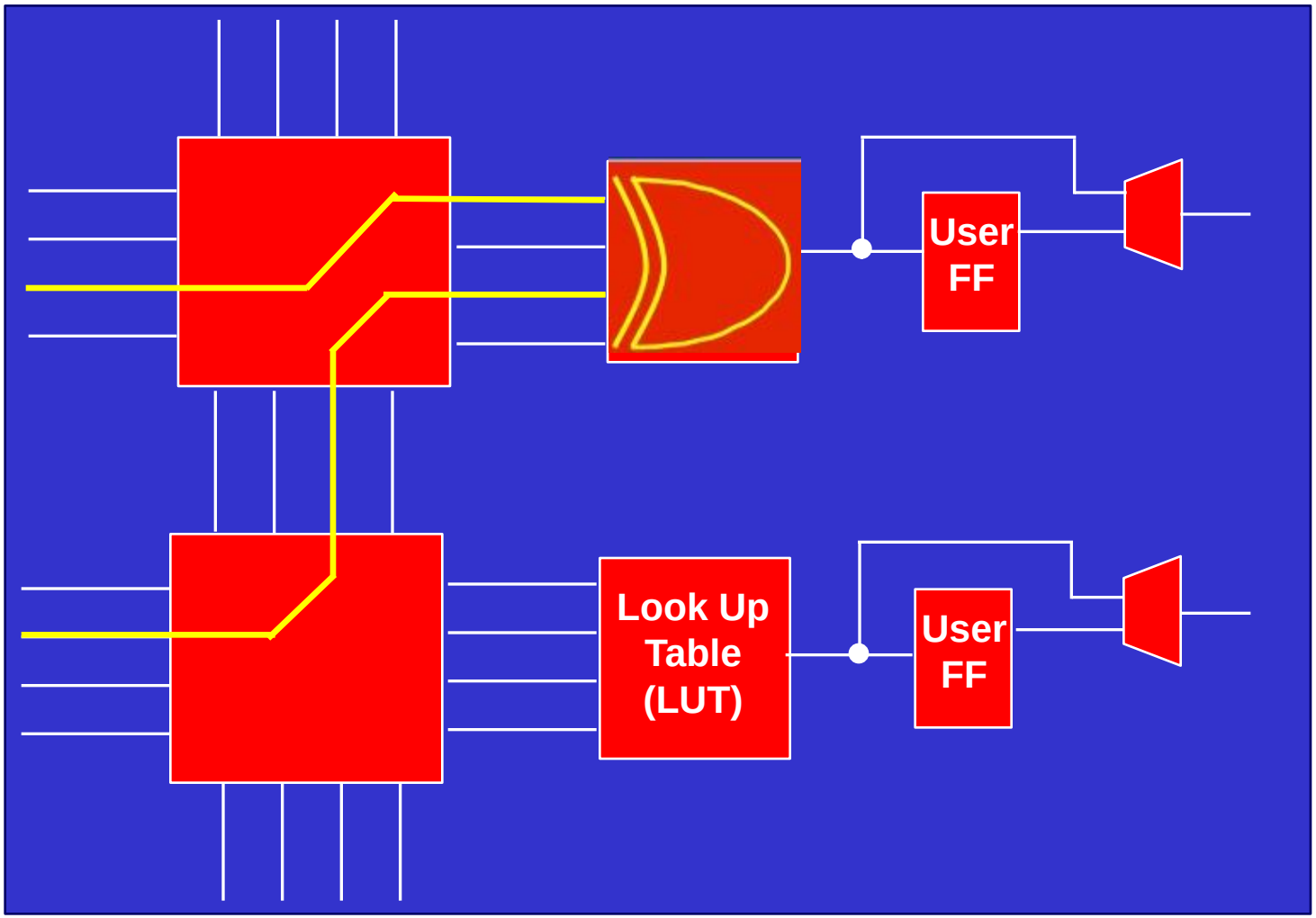
FPGA design



FPGA design – Routing Upset



FPGA design – Logical Upset



SRAM-FPGA SEU Sensitivity

- Heavy Ion cross section (Configuration Memory)
  - σ_{sat}= 5.5 10^{-8} cm^2/bit (Virtex 2)
  - σ_{sat}= 2.5 10^{-7} cm^2/bit (Virtex 4)
- Proton cross section (Configuration Memory)
  - σ_{sat}= 3.8 10^{-14} cm^2/bit (Virtex 2)
  - σ_{sat}= 4.5 10^{-14} cm^2/bit (Virtex 4)
- Estimated Upset Rate (L2 orbit)
  - Normal background **8/d**, Worst Day **1600/d** (XQR2V6000)
  - Normal background **13.46/d**, Worst Day **2908.48/d** (XC4VLX200)
- Design technique for SEU mitigation are essential

A few considerations

- Not all FPGA configuration upsets affect design behavior
- Only "sensitive" configuration bits will cause a design to fail when upset
- Dependent on design style (mitigation technique, density, etc)
- Tools to evaluate design SEU sensitivity are necessary

FLIPPER

- Fault Injection tool to study SEUs in SRAM-FPGAs
  - ESA/ESTEC contract 18559
  - Patent N. 1376923
- The fault model in FLIPPER is the bit-flip of configuration memory cells

CAN WE RELIABLY USE FLIPPER FOR PREDICTION PURPOSES???

Accelerator validation is needed!!!!

FLIPPER Boards

Sample design

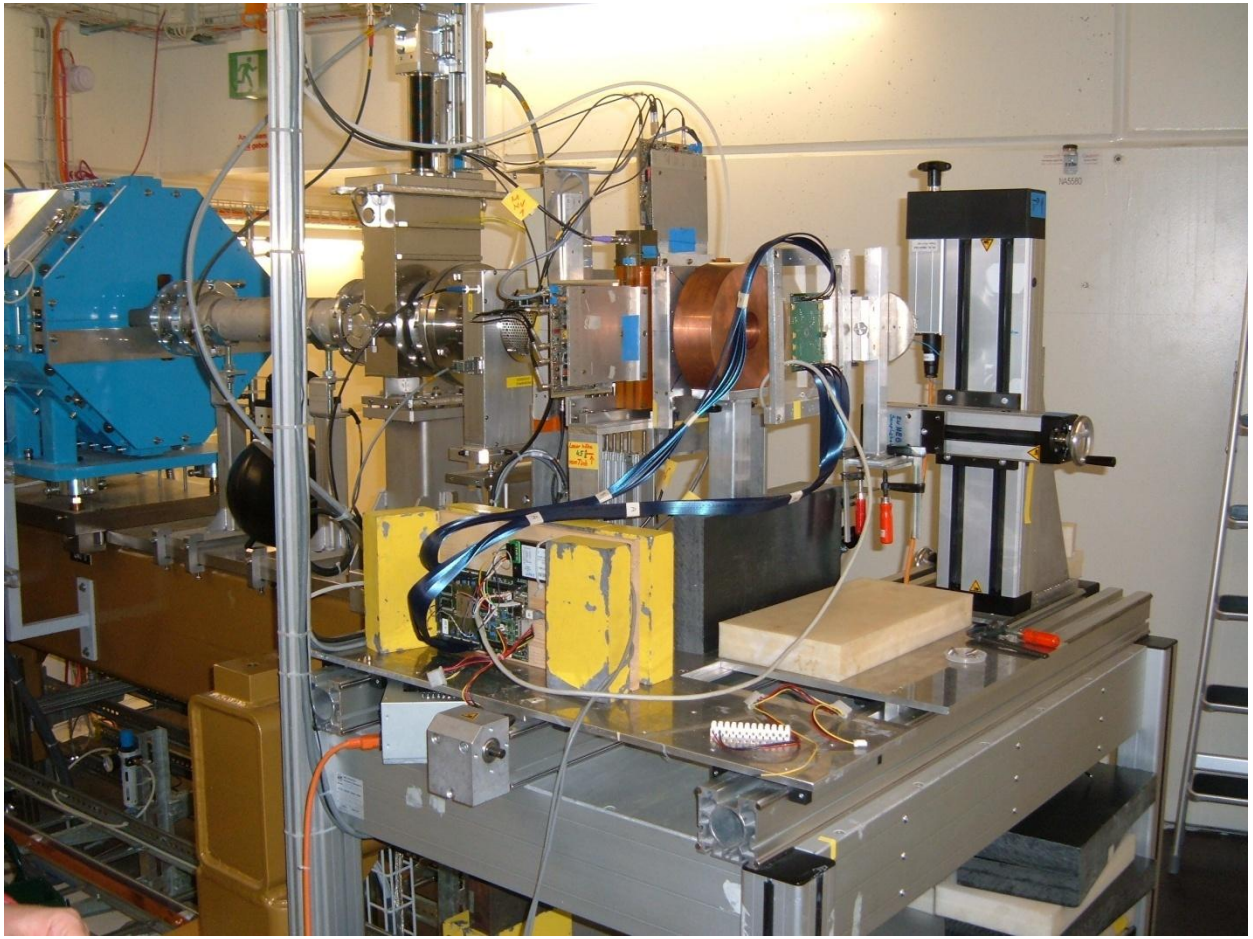
- ESA benchmark design consisting of modules
  - FFT: Fourier Transform of a data matrix
  - MULT16_LUT: 2-stage 16x16 bit multiplier instantiated twice
  - MULT16_MULT18: 10-stage 16x16 bit multiplier instantiated twice (embedded)
  - FFmatrix: two identical copies of a shift register chain (480 bits each)
  - ROMff: two copies of a shift register (256 bit each); the former is loaded and holds the stored values, the latter reads the values stored by the former
- V1 and V2 hardened design variants
  - V1 is derived from the unprotected design by straightly applying the TMRtool.
  - V2 is more robust than V1… In V2 a dummy feedback path, controlled by a multiplexer, is inserted for each flip-flop (the TMRtool is forced to instantiate a voter for every flip-flop in the design)

FI campaign

- Accumulation mode
  - the altered bit is NOT restored before the successive injection is performed
  - mimics the irradiation exp
- Configuration memory bits are flipped according to a random list of memory locations
- About 1000 runs for each variant; predefined maximum number of inj. = 100000

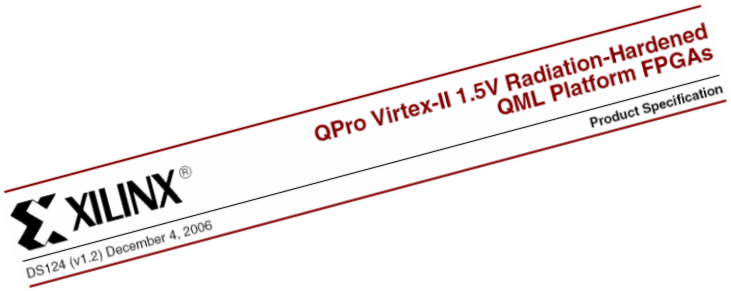
FLIPPER@PSI

PSI, Switzerland, November 23, 2008



Irradiation experiment

DUT Device: XQR2V6000



- 180 MeV proton beam (nominal)
- average flux : ~ $6.3 \cdot 10^{7}$ cm^{-2} s^{-1}
  - 1 CBU at most during test vector application
  - CBU_{rate}: ~ 82 s^{-1}
- stimuli: ~ 28000 vectors@10 MHz
- total exposure time: ~ 8 hours
- Fluence: ~ $2.2 \cdot 10^{12}$ p/cm^{-2}
- TID: < 140 krad
- ~ 600 samples for V2, ~ 400 samples for V1

Radiation Specifications(1)

Table 3: **Minimum Radiation Tolerances**

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019.5, Dose Rate ~50.0 rad(Si)/sec	200	-	krad(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Linear Energy Transfer (LET)	160	-	(MeV-cm²/mg)
SEFI	Single Event Functional Interrupt GEO 36,000km Typical Day		1.5E-6	Upsets/Device/Day

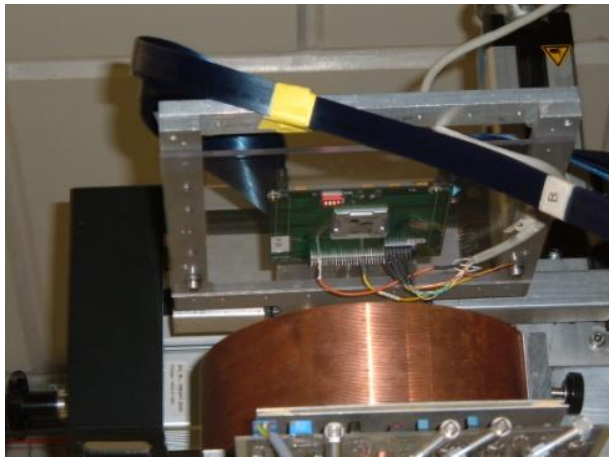
XQR2V6000 : device specification

Device static proton cross section (per bit)

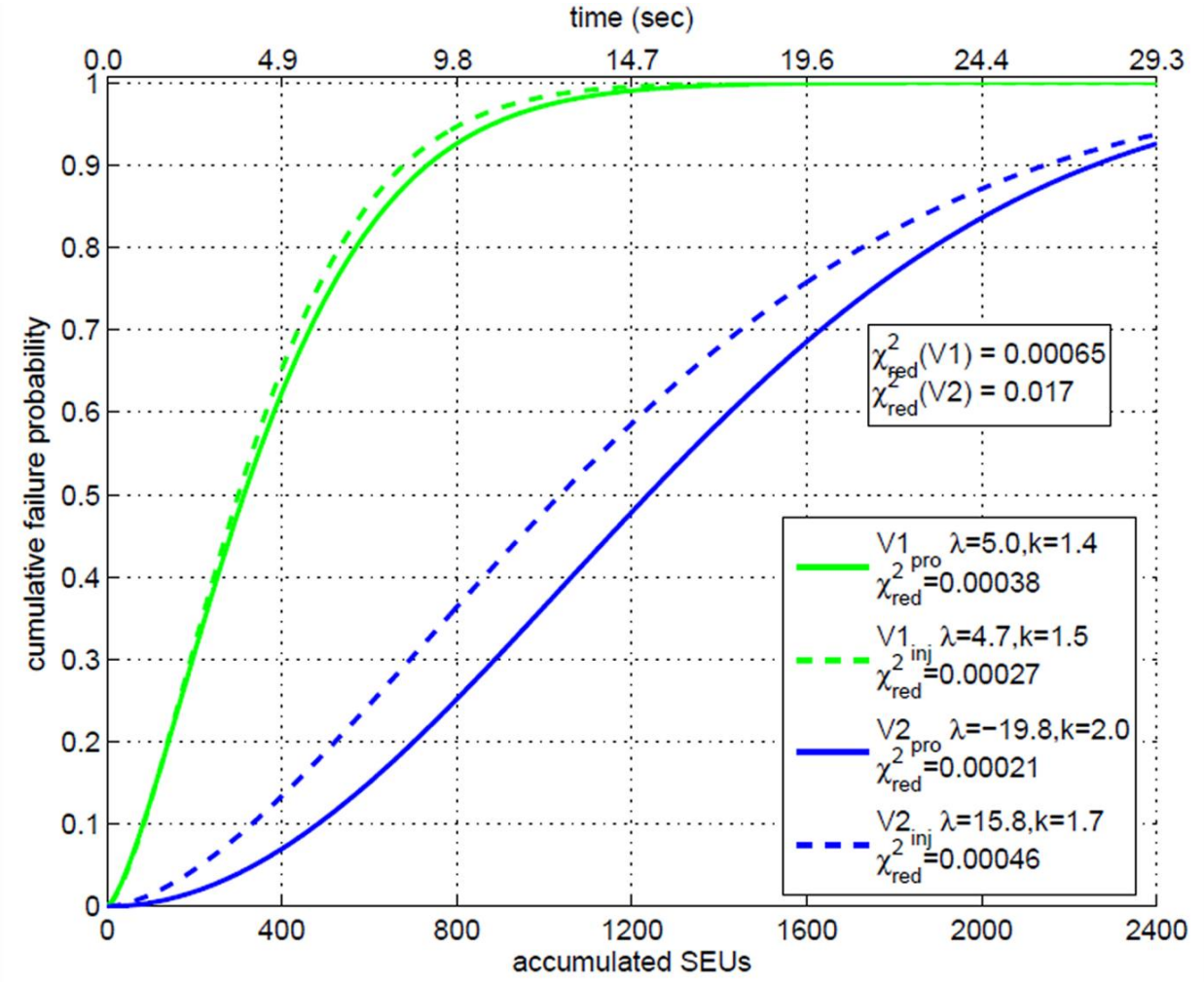
$3 \cdot 10^{-14}$ cm^2 @198 MeV

# of configuration cells

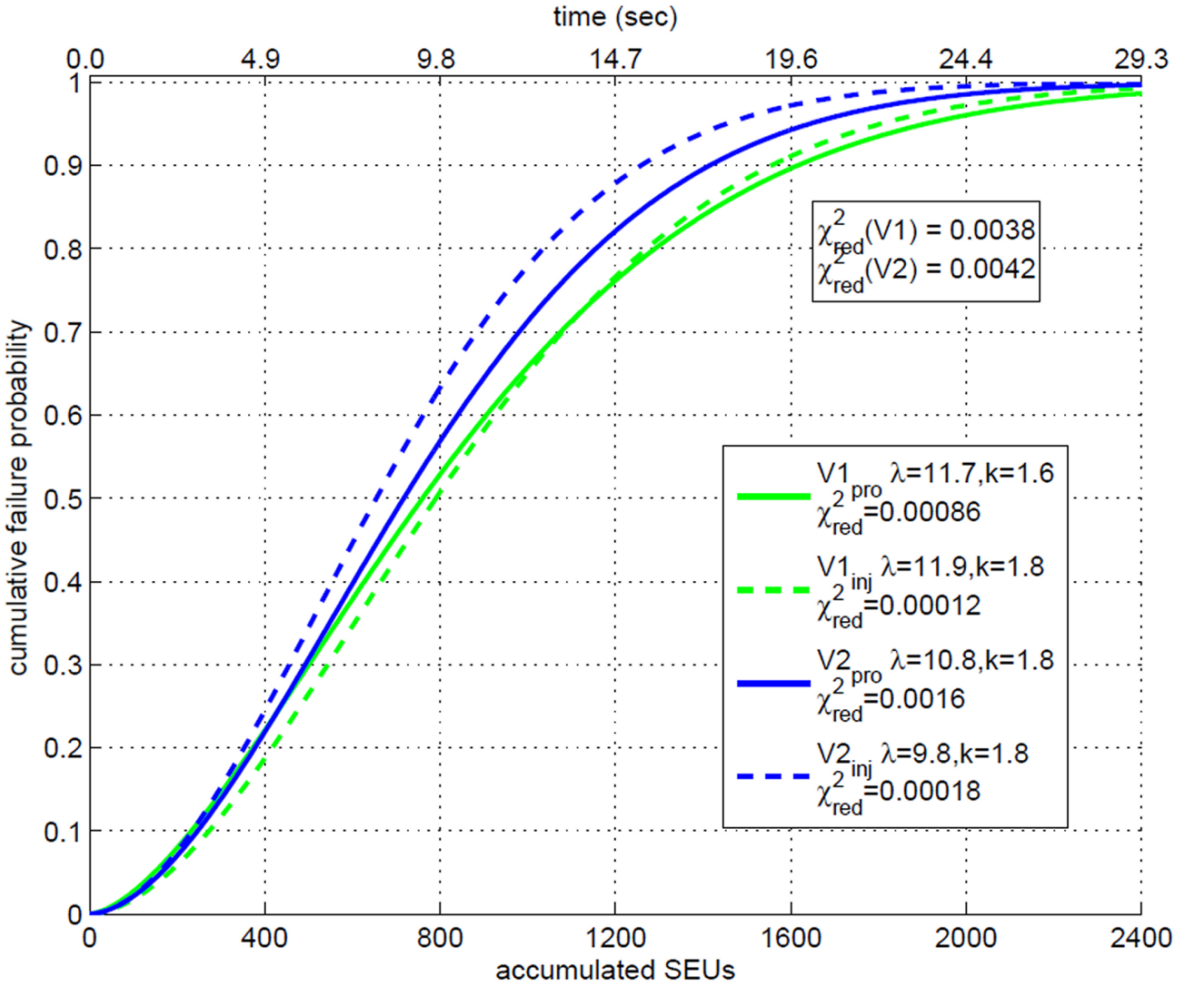
19.742.976



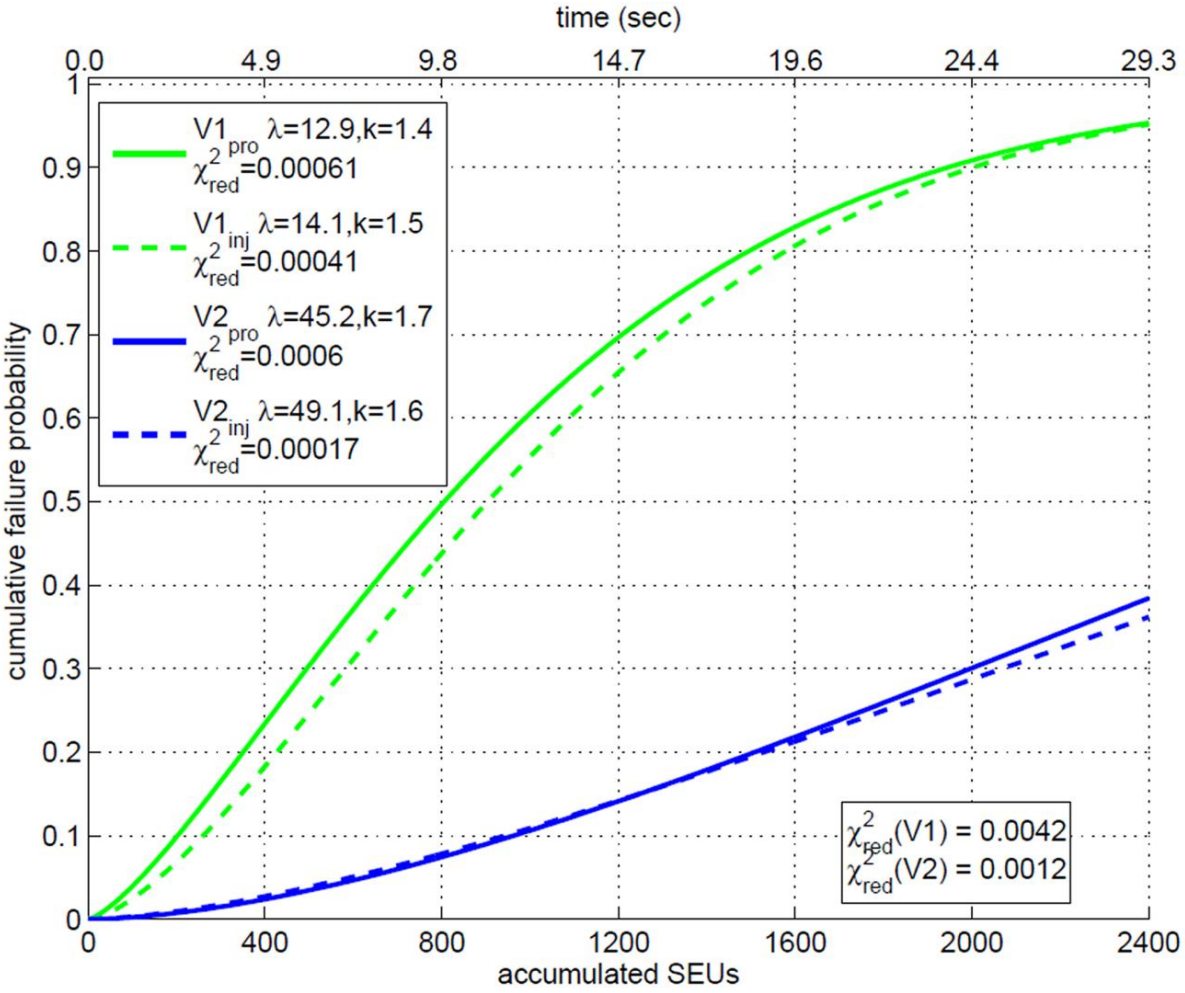
FFmatrix


time (sec)
0.0
4.9
9.8
14.7
19.6
24.4
29.3
cumulative failure probability
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
400
800
1200
1600
2000
2400
accumulated SEUs
χ^2_{red}(V1) = 0.00065
χ^2_{red}(V2) = 0.017
V1 pro λ=5.0,k=1.4
χ^2_{red}=0.00038
V1 inj λ=4.7,k=1.5
χ^2_{red}=0.00027
V2 pro λ=−19.8,k=2.0
χ^2_{red}=0.00021
V2 inj λ=15.8,k=1.7
χ^2_{red}=0.00046

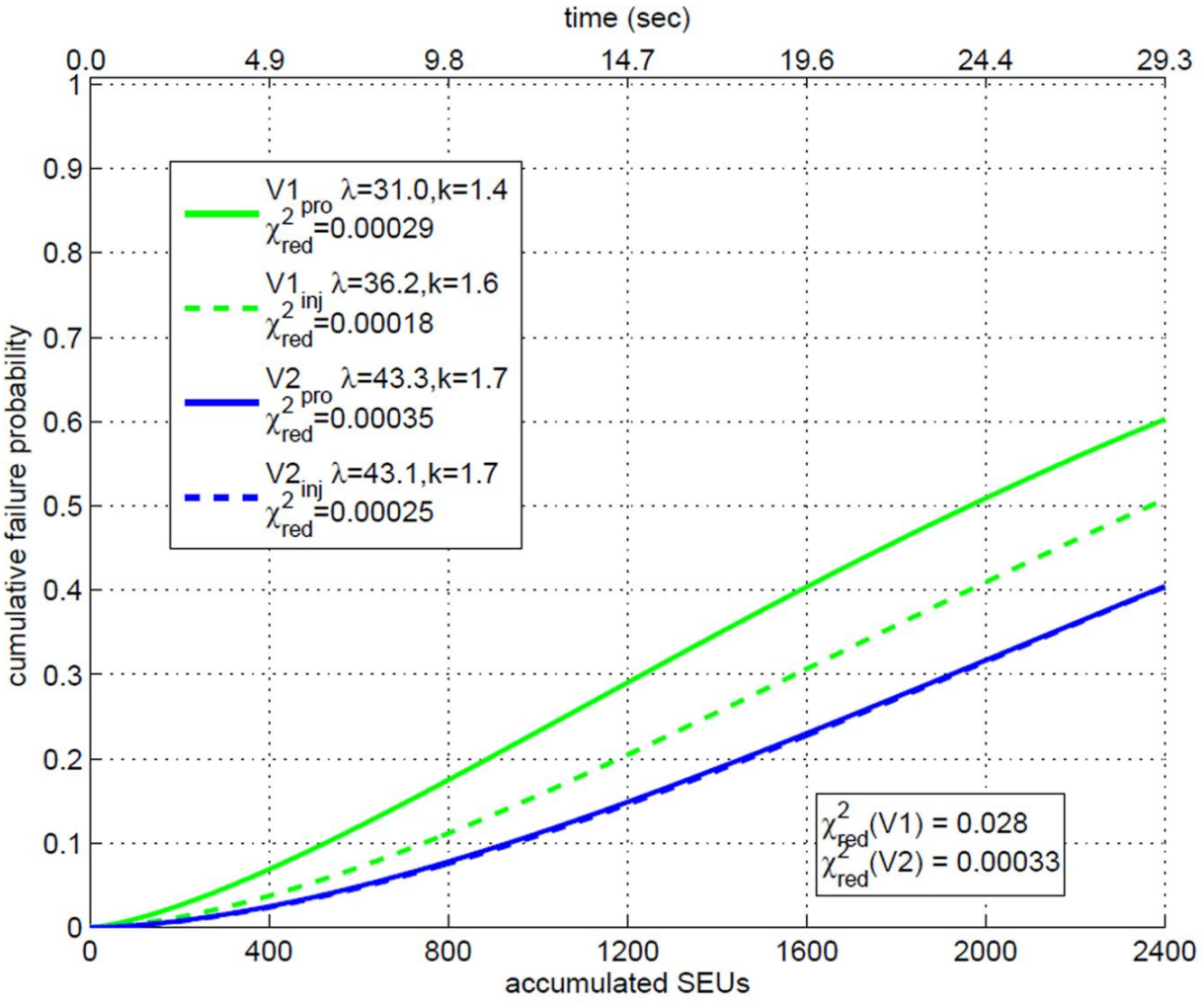
FFT


time (sec)
0.0
4.9
9.8
14.7
19.6
24.4
29.3
cumulative failure probability
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
400
800
1200
1600
2000
2400
accumulated SEUs
χ^2_{red}(V1) = 0.0038
χ^2_{red}(V2) = 0.0042
V1 pro λ=11.7,k=1.6
χ^2_{red}=0.00086
V1 inj λ=11.9,k=1.8
χ^2_{red}=0.00012
V2 pro λ=10.8,k=1.8
χ^2_{red}=0.0016
V2 inj λ=9.8,k=1.8
χ^2_{red}=0.00018

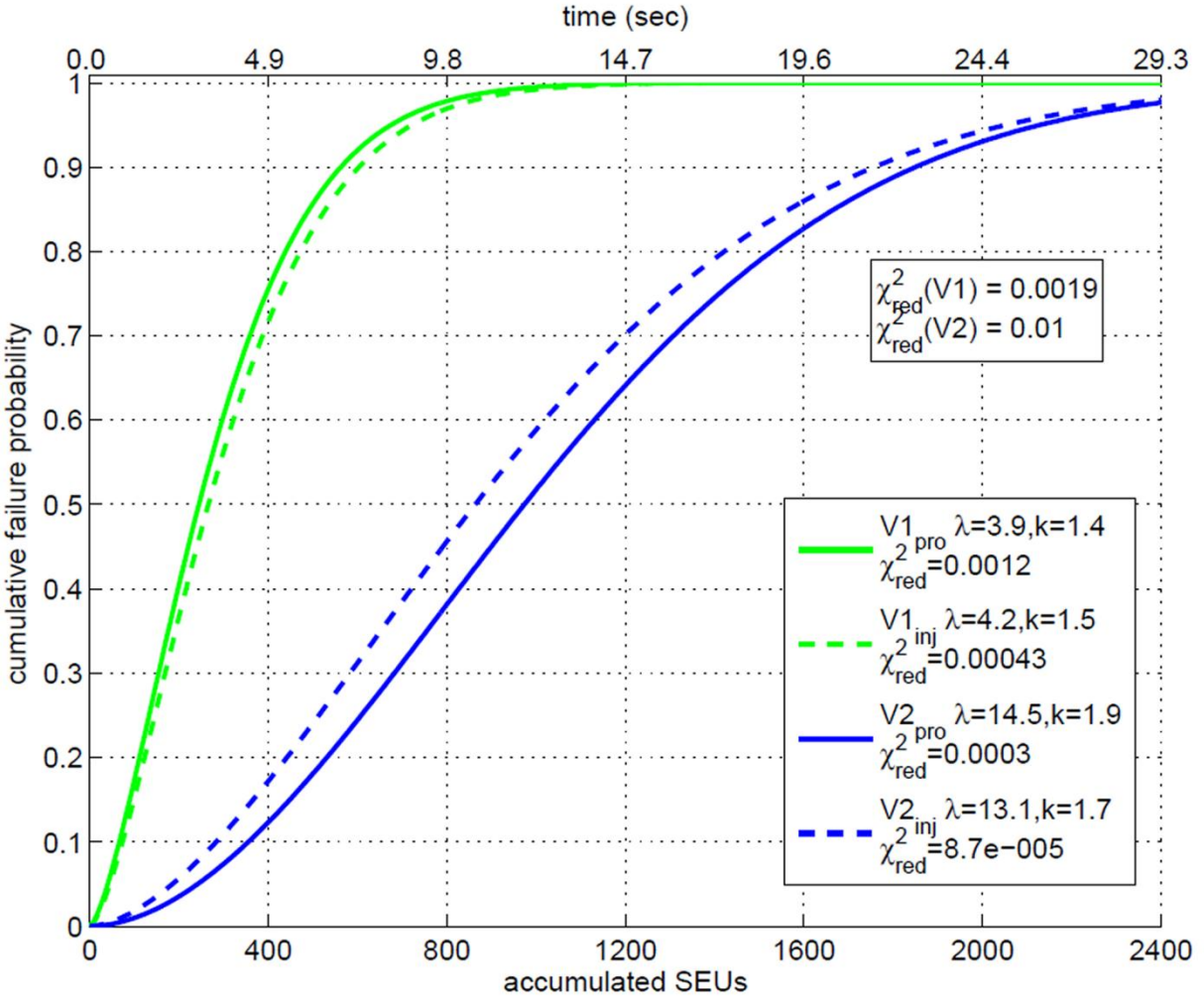
ROMff


time (sec)
0.0
4.9
9.8
14.7
19.6
24.4
29.3
cumulative failure probability
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
V1pro λ=12.9,k=1.4
χ2red=0.00061
V1inj λ=14.1,k=1.5
χ2red=0.00041
V2pro λ=45.2,k=1.7
χ2red=0.0006
V2inj λ=49.1,k=1.6
χ2red=0.00017
χ2red(V1) = 0.0042
χ2red(V2) = 0.0012
0
400
800
1200
1600
2000
2400
accumulated SEUs

Mult16_LUT

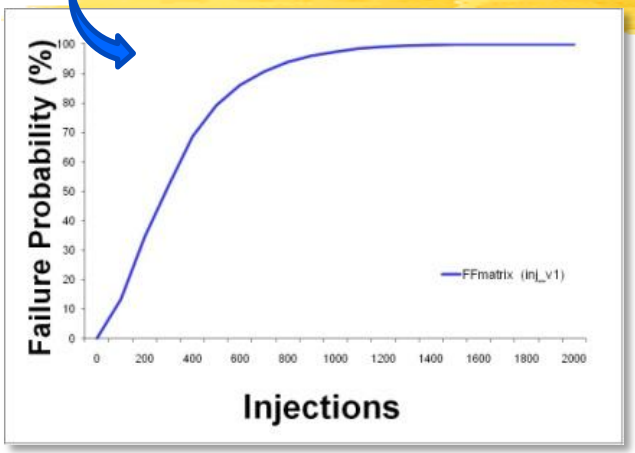

time (sec)
0.0
4.9
9.8
14.7
19.6
24.4
29.3
cumulative failure probability
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
V1pro λ=31.0,k=1.4
χ2red=0.00029
V1inj λ=36.2,k=1.6
χ2red=0.00018
V2pro λ=43.3,k=1.7
χ2red=0.00035
V2inj λ=43.1,k=1.7
χ2red=0.00025
χ2red(V1) = 0.028
χ2red(V2) = 0.00033
0
400
800
1200
1600
2000
2400
accumulated SEUs

Mult16_Mult18



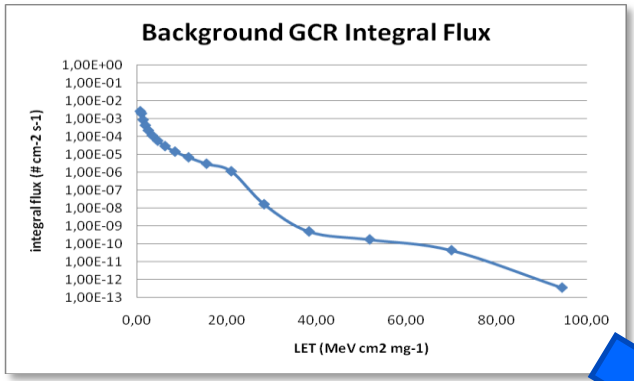
Design Failure Prediction

Design Level

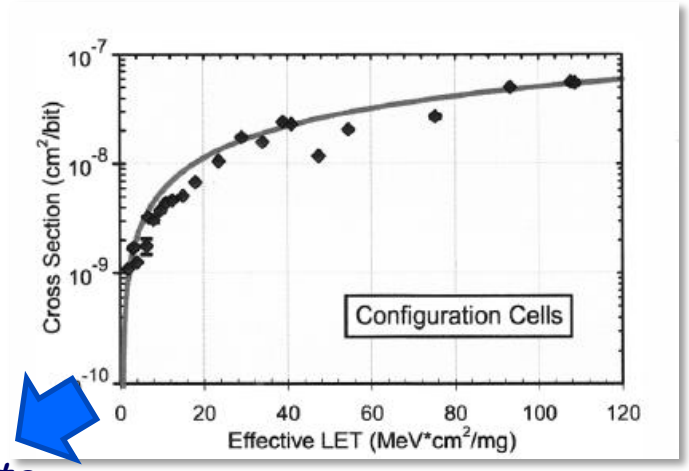


$$t \propto \frac{1}{CBU_{rate}} \cdot n_{inj}$$

Device Level



CBU_{rate}



Thank you!

http://cosy.iasf-milano.inaf.it/flipper_index.htm

Weibull

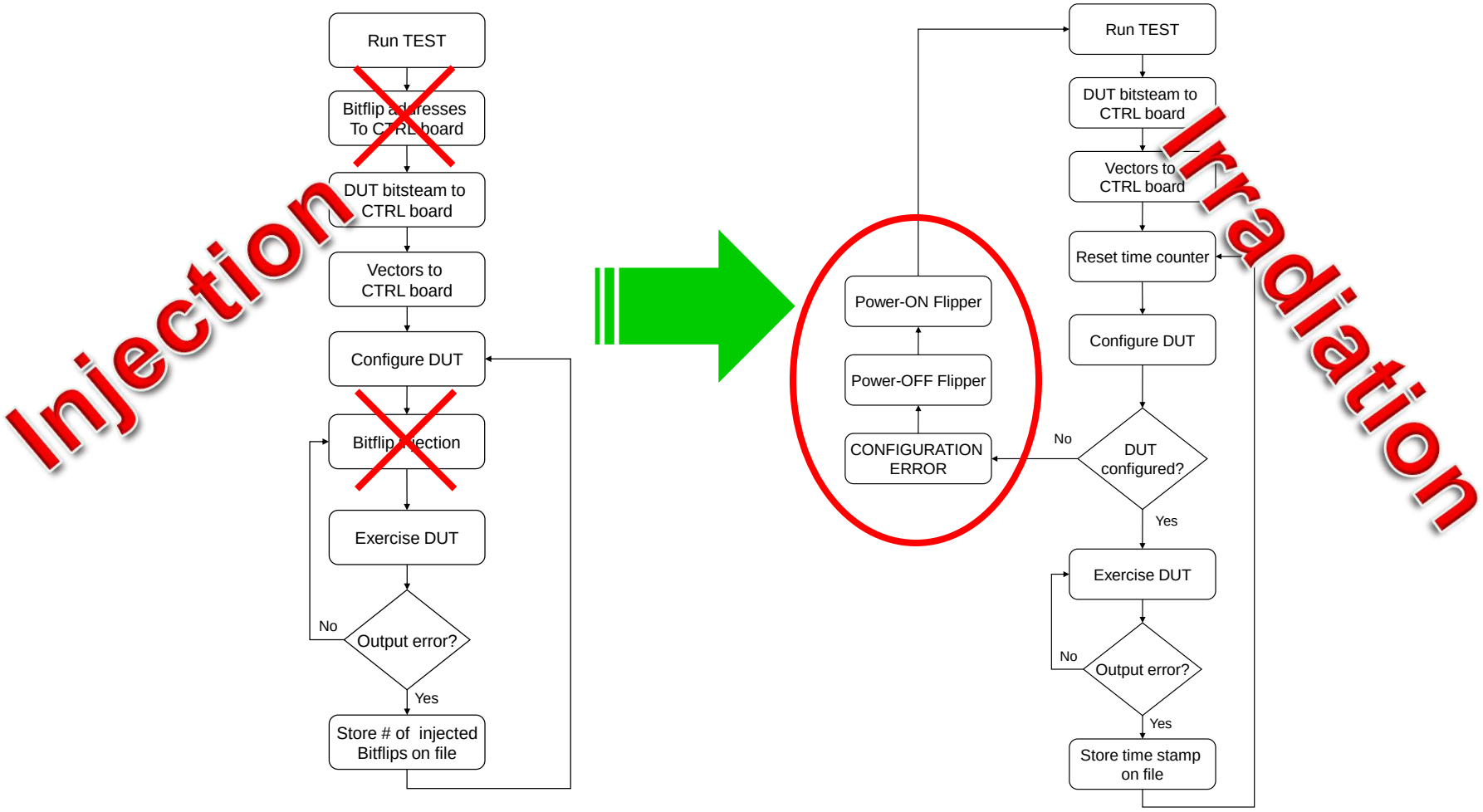
$$F(x;k,\lambda) = 1 - \exp\left(-\left(\frac{x}{\lambda}\right)^{k}\right)$$

$k > 0$ shape parameter

$\lambda > 0$ scale parameter

$$\chi^2_{red} = \frac{1}{DOF}\sum_{k=1}^{n}\frac{(O_k - E_k)^2}{E_k}$$

Procedures


Injection
Run TEST
Bitflip addresses To CTRL board
DUT bitsteam to CTRL board
Vectors to CTRL board
Configure DUT
Bitflip injection
Exercise DUT
Output error?
No
Yes
Store # of injected Bitflips on file
Irradiation
Run TEST
DUT bitsteam to CTRL board
Vectors to CTRL board
Reset time counter
Configure DUT
DUT configured?
No
Yes
Exercise DUT
Output error?
No
Yes
Store time stamp on file
CONFIGURATION ERROR
Power-OFF Flipper
Power-ON Flipper

FLIPPER

- FLIPPER injects bit-flip faults within the FPGA configuration memory by means of partial re-configuration
- The system consists of a hardware platform and a software application running on a PC
- DUT device is an XQR2V6000 device hosted on a piggy-back board, stacked on the control board
- Test vectors and reference values for the functional test of implemented designs are imported by the software application from an external HDL simulator